**Computer Organization and Architecture**

**ETCS - 204**

**TUTORIAL 1**

1. The following transfer statements specify a memory. Explain a memory operation in each case:
2. M[AR] ­­­­­­­­­­­­­­­­­­­­­­­­------🡪 R3
3. R2 -----🡪M[AR]
4. In order to execute a program, instructions must be transferred from memory along a bus to the CPU. If the bus has 8 data lines, at most one 8 bit byte can be transferred at a time. How many memory accesses would be needed in this case to transfer a 32 bit instruction from memory to the CPU?
5. A computer has 16 register, an ALU with 32 operations and a shifter with eight operations all Connected to a common bus system. (i) Formulate a control word for a micro operation. (ii) Specify the number of pits in each field on the control word and give a general encoding scheme.
6. Identify the number of address lines needed for interfacing 8KB memory.
7. Specify the number of registers and memory cells required in a 128 x 4 memory chip?

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**TUTORIAL 2**

1. A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.

(i) How many selection inputs are there in each multiplier?

(ii) What sizes of multiplexers are needed?

(iii) How many multiplexers are there in the bus?

1. We need to load the accumulator with the value as 28h. This value is stored at 2082h memory location. Write the assembly code to implement it.
2. Design an arithmetic circuit with one selection variable S and two n-bit data inputs A & B. The circuit generates the following four arithmetic operations in conjunction with the input carry Cin. Draw the logic diagram for the first two stages.
3. Specify the contents of the registers and the flag status as the following instructions are executed.
4. MVI A, 00H
5. MVI B, F8H
6. MOV C, A
7. MOV D, B
8. HLT
9. Write instructions to load the hexadecimal number 65H in register C and 92H in accumulator A. Display the number 65H at PORT0 and 92H at PORT1.

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**TUTORIAL 3**

1. Explain the outcome of the instruction LXI H, 4600h and LHLD 4600h.

1. Specify the contents of the registers and the flag status as the following instructions are executed.
2. Write instructions to load the hexadecimal number 65H in register
3. Write the machine instructions required to execute the following arithmetic instructions

W=(A+B-C+(D\*E-F))/(G+H\*K)\*J/L

1. Describe the difference between the instructions LDA 2437H and LHLD 2437H.

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**TUTORIAL 4**

1. An instruction is stored at location 300 with its address field at location 301. The address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is
2. Direct
3. Immediate
4. Relative
5. Register indirect
6. Index
7. If we add 87H and 79H in 8085 microprocessor, specify the contents of the accumulator and the status of the S, Z, and CY flag?
8. Describe the difference between the instructions LDA 2437H and LHLD 2437H.
9. **Write an assembly code that will store the contents of an accumulator and flag register at locations 2000h and 2001h.**
10. How many bits wide memory address have to be if the computer had 16 MB of memory? (use the smallest value possible).

**Tutorial No – 5**

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1. How can you explain the phases of an Instruction cycle?

2. Compare BUN and BSA using an example?

3. Design the control function to execute ISZ instruction?

4. Draw the timing diagram of the following Instruction:

(i) D3 T4: SC ← 0

(ii) D2 T5: AC ← DR, SC ← 0

5. Compare MRI, RRI, and IORI by illustrating some examples?

6. Discuss the process of implementing a control unit?

**Tutorial No – 6**

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1. Define the terms in your own words: Micro-Program, Micro-Instruction, Micro-Operation, Micro-Code, and Control Memory?

2. Compare Hardwired and Micro programmed Control Unit?

3. Design a simple CPU which executes ADD, AND, JMP, and INC instructions?

4. Design the simple ALU that can perform ADD, SUB, AND, OR, INC, DEC?

5. A computer uses a memory unit with 256 K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part.

(a) How many bits are there in the operation code, the register code part, and the address part?

(b) Draw the instruction word format and indicate the number of bits in each part.

(c) How many bits are there in the data and address inputs of the memory?

6. An output program resides in memory starting from address 2300. It is executed after the computer recognizes an interrupt when FGO becomes a 1 (while IEN = 1).

(a) What instruction must be placed at address 1?

(b) What must be the last two instructions of the output program?

**Tutorial No – 7**

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1. How Michael J Flynn classified the computer systems?

2. In how many ways a number can be represented in computer system. Explain with example?

3. A computer has 32 bit instructions and 12 bit addresses. If there are 250 two-address instructions, how many one-address instructions can be formulated?

4. Design a General Register Organization to implement R1 ← R4 ^ R5?

5. A two word instruction is stored in memory at an address designated by symbol W. The address field of the instruction (stored at W + 1) is designated by the symbol Y. The operand used during the execution of the instruction is stored at an address symbolized by Z. An index register contains the value X. State how Z is calculated from the other addresses if the addressing mode of the instruction is

(a) Direct (b) Indirect

(c) Relative (d) Indexed

6. Write a program to evaluate arithmetic expression

X = (A – B) \* (((C – D \* E)/F)/G)

(a) Using a general register computer with three address instructions.

(b) Using a general register computer with two address instructions.

(c) Using an accumulator type computer with one-address instructions.

(d) Using stack organized computer with zero address instructions.

7. Justify the statement “stack computer consists of an operation code only with no address field.”

**Tutorial No – 8**

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1. Is there any Hazards in Pipeline processing? If yes, how can you avoid these hazards?

2. Differentiate between Write Back and Write Through System?

3. In certain scientific computations it is necessary to perform the arithmetic operation

(Ai + Bi) (Ci + Di) with a stream of numbers. Specify a pipeline configuration to carry out this task. List the contents of all registers in the pipeline for i = 1 through 6.

4. A non-pipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved ?

5. Perform the arithmetic operations below with binary numbers and with negative numbers in signed-2’s complement representation. Use seven bits to accommodate each number together with its sign.

In each case, determine if there is an overflow by checking the carries into and out of the sign bit position.

1. (+35) + (+40) (b) (–35) + (–40).

6. Prove that the multiplication of two n-digit numbers in base r gives a product no more than 2n digits in length. Show that this statement implies that no overflow can occur in the multiplication operation.

**Tutorial No – 9**

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1. What are the memory performance parameters?

2. Compare memory mapped I/O vs I/O mapped I/O.

3. Consider a cache consisting of 128 blocks of 16 words each for a total of 2048, (2k)

words, and assume that the main memory is addressable by a 16 bit address and it consists of 4k blocks. How many bits are there is each of the Tag, Block/Set and word fields for different mapping techniques.

4. The logical address space in a computer system consists of 128 segments. Each segment can have up to 32 pages of 4 K words in each. Physical memory consists of 4 K blocks of 4 K words in each. Formulate the logical and physical address formats.

5. How many characters per second can be transmitted over a 1200-baud line in each of the following modes? (Assume a character code of eight bits).

(a) Synchronous serial transmission.

(b) Asynchronous serial transmission with two stop bits.

(c) Asynchronous serial transmission with one stop bit.

6. A DMA controller transfers 16-bit words to memory using cycle stealing. The words are assembled from a device that transmits characters at a rate of 2400 characters per second. The CPU is fetching and executing instructions at an average rate of 1 million instructions per second. By how much will the CPU be slowed down because of the DMA transfer?